Product/Process Change Notice - PCN 14_0218 Rev. -

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This notice is to inform you of a change that will be made to certain ADI products (see Appendix A) that you may have purchased in the last 2 years. **Any inquiries or requests with this PCN (additional data or samples) must be sent to ADI within 30 days of publication date.** ADI contact information is listed below.

PCN Title: AD9559 Die Revision

Publication Date: 30-Jan-2015

Effectivity Date: 30-Apr-2015 *(the earliest date that a customer could expect to receive changed material)*

Revision Description:

Initial Release

Description Of Change

Circuitry has been added to improve functionality and fix 9 issues:
1. A reset on the RF Divider was added to ensure that the RF Divider always powers up in a known state.
2. The state machine that interfaces with the EEPROM was redesigned to ensure EEPROM data is properly loaded.
3. Synchronization circuitry was implemented that properly syncs the SDM on the correct phase of the internal clock on exit of power-down state.
4. The internal clock relationships were properly gated between the TDCs and System Clock in order to ensure proper DPLL startup.
5. The DPLL divider was limited to 23 bits in Frac/Mod (rather than 24-bits), so a register was modified to handle the sign-bit correctly.
6. VCO calibration fixes to prevent APLL calibration failure and enhance the accuracy of the calibration.
7. APLL VCO voltage regulator design changed to allow more margin over temp with less jitter variation.
8. Power-on Reset Enhanced and logic added to accurately detect the presence of the 1.8V and 3.3v power supplies.
9. APLL lock detector changed to avoid false "loss of lock" indication.

Reason For Change

Items 1-4: The RF Divider, EEPROM interface, SDM timing, and DPLL start-up were not functionally robust.
Item 5: In the case of the DPLL divider, the device was originally intended to have a 24-bit fractional divider.
Item 6: The APLL calibration fails in a very small number of cases on existing silicon, requiring to user to reissue a calibration.
Item 7: To enhance the robustness of the part over temperature and guarantee more consistent jitter performance.
Item 8: To ensure that both the 3.3V and 1.8V supplies are accurately detected before issuing POR (power-on reset). In rare cases, if the 1.8V and 3.3V supplies ramped at different times, current leakage through the ESD structure would cause the monitoring circuit to falsely declare both power supplies as present.
Item 9: The APLL lock detector on AD9554 (4-channel DPLL) occasionally (but rarely) indicated a false loss of lock. The same fix on the AD9554 has been applied to the AD9559 APLL lock detector as a precaution.

Impact of the change (positive or negative) on fit, form, function & reliability

There is no change to either the fit or the form for nearly all AD9559 applications.

For Item #1, In the rare cases where the user wishes to change the RF Divider setting without reissuing an APLL recalibration, the user should check Revision D of the AD9559 datasheet for details on how to so. However, nearly all AD9559 applications will not require any modification to the device programming.

Functionality of the DPLL 24-bit fractional divider has been corrected to match the original design objective of the part.

Reliability of the RF Divider, EEPROM interface, SDM timing, and DPLL start-up has improved.

Product Identification *(this section will describe how to identify the changed material)*

Read-only Register 0x000A will have the value of 0x30.

Previous versions will have a value < 0x30 in Register 0x000A

Additionally, marking slightly changed to contain complete part number all on one line.

Summary of Supporting Information

Qualification will be performed per ADI0012, Procedure for Qualification of New or Revised Processes. See attached Qualification Plan.

Supporting Documents

Attachment 1: Type: Qualification Plan

ADI_PCN_14_0218_Rev_-_AD9559_Die_Revision_PCN_Qual_Table.pdf

For questions on this PCN, please send an email to the regional contacts below or contact your local ADI sales representatives.					
Americas:	PCN_Americas@analog.com	**Europe:**	PCN_Europe@analog.com	**Japan:**	PCN_Japan@analog.com
				Rest of Asia:	PCN_ROA@analog.com

Appendix A - Affected ADI Models				
Added Parts On This Revision - Product Family / Model Number (2)				
AD9559 / AD9559BCPZ	AD9559 / AD9559BCPZ-REEL7			

Appendix B - Revision History			
Rev	**Publish Date**	**Effectivity Date**	**Rev Description**
Rev. -	30-Jan-2015	30-Apr-2015	Initial Release